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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,910	01/28/2002	Keshab K. Parhi	1875.2100000	1490

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EXAMINER	
YANG, LINA	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,910	PARHI, KESHAB K.	
	Examiner	Art Unit	
	Lina Yang	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2002*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-20* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application is in condition for allowance except for the following formal matters:

Fig. 22 is objected since the element 2206 is simply the whole block copy of claim 1, which does not help to understand the claimed subject matter. A flowchart is supposed to offer a simple easy way to understand/explain the claimed subject matter.

The term "n-level" recited in all independent claims (claims 1, 10 and 16) need to be defined in certain range. One suggestion would be "wherein, n is an integer and n is greater than and equal 2".

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Keyboard

Allowable Subject Matter

1. Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance.

The subject matter of claims 1-9 is allowable over prior art of record, because all prior arts fail to teach or suggest a digital logic circuit for determining an output value

converts the plurality of input values to a plurality of intermediate values; ***a plurality of multiplexers each having a first and a second input port, an output port, and a control port, the plurality of multiplexers arranged to form a pipelined multiplexer loop having at least a first and a second stage, the first stage consisting of a first multiplexer, and the second stage consisting of a second and a third multiplexer, the pipelined multiplexer loop being coupled to the n-level look-ahead network***; a first communications link that couples the output port of the second multiplexer to the first input port of the first multiplexer; a second communications link that couples the output port of the third multiplexer to the second input port of the first multiplexer; a first feedback loop that couples the output port of the first multiplexer to the control port of the first multiplexer, the first feedback loop comprising a first delay device having a first delay time; and a second feedback loop that couples the output port of the first multiplexer to the control ports of the second and third multiplexers, the second feedback loop comprising the first delay device and a second delay device having a second delay time, wherein ***the first delay time is an integer multiple of the second delay time and is equal to (n+1) times a clock period of operation of the digital logic circuit,*** as recited in the claims.

The subject matter of claims 10-15 is allowable over prior art of record, because all prior arts fail to teach or suggest a digital logic circuit for determining an output value based on a plurality of inputs values, comprising: ***an n-level look-ahead network that converts the plurality of input values to a plurality of intermediate values; a***

plurality of multiplexers each having a first and a second input port, an output port, and a control port, the plurality of multiplexers arranged to form a pipelined multiplexer loop, the pipelined multiplexer loop being coupled to the n-level look-ahead network; a first communications link that couples the output port of a first multiplexer to the first input port of a second multiplexer; a second communications link that couples the output port of a third multiplexer to the second input port of the second multiplexer; a first feedback loop that couples the output port of the second multiplexer to the control port of the second multiplexer, the first feedback loop comprising a first delay device having a first delay time; and a second feedback loop that couples the output port of the second multiplexer to the control ports of the first and third multiplexers, the second feedback loop comprising the first delay device and a second delay device having a second delay time, ***wherein the first delay time is an integer multiple of the second delay time and is equal to (n+1) times a clock period of operation of the digital logic circuit***, as recited in the claims.

The subject matter of claims 10-15 is allowable over prior art of record, because all prior arts fail to teach or suggest a method for pipelining multiplexer loops that form part of an integrated circuit, the method comprising the steps of: (a) selecting a number of input values to be provided to a pipelined multiplexer loop during a clock period of operation of the integrated circuit; (b) selecting a number of look-ahead steps to be implemented as a part of the pipelined multiplexer loop; and (c) implementing the pipelined multiplexer loop using at least one digital logic circuit, comprising: ***an n-level***

look-ahead network that converts the number of input values selected in step (1) to a plurality of intermediate values, wherein n represents the number of look-ahead steps selected in step (2), a plurality of multiplexers each having a first and a second input port, an output port, and a control port, the plurality of multiplexers arranged to form the pipelined multiplexer loop, the pipelined multiplexer loop having at least a first and a second stage, the first stage consisting of a first multiplexer, and the second stage consisting of a second and a third multiplexer, the pipelined multiplexer loop being coupled to the n-level look-ahead network, a first communications link that couples the output port of the second multiplexer to the first input port of the first multiplexer, a second communications link that couples the output port of the third multiplexer to the second input port of the first multiplexer, a first feedback loop, having a first delay time, that couples the output port of the first multiplexer to the control port of the first multiplexer, and a second feedback loop, having a second delay time, that couples the output port of the first multiplexer to the control ports of the second and third multiplexers, ***wherein the first delay time is an integer multiple of the second delay time and is equal to (n+1) times a clock period of operation of the integrated circuit***, as recited in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Azadet et al. (U.S. Patent No. 6,192,072 B1) discloses a method and an apparatus for increasing the effective processing speed of a parallel decision-feedback equalizer (DFE) by combining block processing and look-ahead techniques in the selection (multiplexing) stage. More specifically, the invention extends a parallel DFE by using look-ahead techniques in the selection stage to precompute the effect of previous blocks on each subsequent block, and to thereby remove the serial output dependency. The parallel DFE includes a multiplexor tree structure that selects an appropriate output value for each block and precomputes the effect of previous blocks on each subsequent block. A multiplexing delay algorithm on the order of logN is employed to resolve the output dependency and thus speeds up parallel block processing DFEs.

Azadet et al. (U.S. Patent No. 6,363,112 B1) discloses that a parallel processing decision feedback equalizer is configured to receive a plurality of symbol blocks in parallel via a plurality of corresponding input branches. It is further configured to generate a plurality of decision samples. The equalizer comprises an input buffer for storing calculated decision samples corresponding to at least one previously received

symbol block and a plurality of tapped delay calculators coupled to the input buffer and located in each of the input branches which are configured to calculate the first portion of a decision feedback signal corresponding to each input branch based on the impulse response samples and the decision samples stored in said input buffer. Azadet et al. further teaches that a plurality of look-ahead-processors located in each one of the input branches and is coupled to a corresponding one of the tapped delay calculators. Each look-ahead-processor has a depth equal to the sequence order of its corresponding branch so as to calculate all possible components of a decision feedback signal for the corresponding branch. A plurality of selectors are coupled to the look-ahead processors so as to select appropriate ones of the possible components of the decision feedback signal based on decision samples obtained from previous branches.

Agazzi et al. (U.S. Patent Application Publication No. 20010035994 A1) discloses a Various systems and methods related to equalization precoding in a communications channel are disclosed. In one implementation preceding is performed on signals transmitted over an optical channel. In one implementation preceding and decoding operations are performed in parallel to facilitate high speed processing in relatively low cost circuits. Initialization of the precoders may be realized by transmitting information related to the characteristics of the channel between transceiver pairs.

Birru (U.S. Patent Application Publication No. 20020181575 A1) discloses a decision feedback equalizer (DFE) includes a forward equalizer, first and second

adders, a decision device, a feedback equalizer, and an N-tap filter. More specifically, the first and second adders, the decision device, and the feedback equalizer constitute a first feedback loop, the second adder, the decision device, and the N-tap filter constitute a second feedback loop. In that case, the second feedback loop is free of an implementation delay associated with the first feedback loop. In the exemplary DFE, N is a positive integer. If desired, the N-tap filter is implemented in fast logic. A method for controlling a decision feedback equalizer based on first and second feedback signals is also described.

Greiss et al. (U.S. Patent Application Publication No. 20020021767 A1) discloses a digital bas-bans receiver. The equalization section has a unique pipeline architecture, enabling it to operate at substantially faster clock rates, and with substantially fewer components, compared to equalizers known in the art. More specifically, the equalization section comprises both forward equalization and decision feedback equalization stages on a common pipeline, with multiplicative coefficients determined using an adaptive process, preferably a least mean squares adaptation. Preferably, clock recovery from the incoming signal is performed by measuring differences between two or more of the coefficients evaluated in the equalization section, using the differences to give substantially better clock recovery for weaker signals than methods at present known in the art. Most preferably, differences are measured between one coefficient in the decision feedback equalization stage, and one coefficient in the forward equalization stage.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lina Yang whose telephone number is (571)272-3151. The examiner can normally be reached Monday through Wednesday between 7:00 a.m. and 7:30 p.m. eastern standard time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 517-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LY

ALPUS H. HSU
PRIMARY EXAMINER